

L Number	Hits	Search Text	DB	Time stamp
1	78	(((((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer)	USPAT; US-PGPUB	2003/05/30 12:14
2	3	((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	EPO; JPO; DERWENT; IBM_TDB	2003/05/30 12:19
3	0	((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	EPO; JPO; DERWENT; IBM_TDB	2003/05/30 12:19
4	28	((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	USPAT; US-PGPUB	2003/05/30 12:26
5	24	((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer))	USPAT; US-PGPUB	2003/05/30 12:20
6	4	((sputter or sputtering) with cleaning with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	USPAT; US-PGPUB	2003/05/30 12:27
7	0	((sputter or sputtering) with cleaning with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer))	USPAT; US-PGPUB	2003/05/30 12:27
8	82	((sputter or sputtering) with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	USPAT; US-PGPUB	2003/05/30 12:27
9	73	((sputter or sputtering) with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer))	USPAT; US-PGPUB	2003/05/30 12:27
10	59	((sputter or sputtering) with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer))) and (cleaning or etching)	USPAT; US-PGPUB	2003/05/30 12:27

11	48	((((((sputter or sputtering) with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer)))) and (cleaning or etching)) and @ad<=20010510	USPAT; US-PGPUB	2003/05/30 12:28
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US-PAT-NO:

6294458

DOCUMENT-IDENTIFIER:

US 6294458 B1

TITLE:

Semiconductor device adhesive layer structure and  
process for forming structure

----- KWIC -----

Application Filing Date - AD (1):

20000131

Brief Summary Text - BSTX (6):

A first level interconnect is then formed overlying the interlevel dielectric (ILD) layer and the conductive plug. The first level interconnect can be formed using a combination of trench and polishing processes or, alternatively, using a combination of patterning and **etching** processes. If the first level interconnect is formed using copper, a barrier may be formed adjacent to the first level interconnect to reduce the migration of copper into surrounding materials. The first level interconnect is formed, for example, as a single inlaid structure. As such, the first level interconnect is created by first depositing a portion of a second ILD which is then etched to form a trench in which the material that makes up the first level interconnect is deposited. Once deposition of the first level interconnect occurs, a polishing process removes any excess material that remains outside of the trench formed.

Brief Summary Text - BSTX (10):

In a conventional inlaid process forming an interconnect structure, a trench is formed in an interlevel dielectric (ILD) layer. The ILD layer is typically silicon dioxide (SiO<sub>2</sub>), doped silicon dioxide, an organic polymer, or some other dielectric material. A way of forming the SiO<sub>2</sub> ILD is CVD or PECVD processes using tetraethoxysilane or alternatively a process using tetraethoxysilane in combination with a fluorine source to form fluorine containing SiO<sub>2</sub> (FTEOS). In order to provide a barrier for the next metal layer on the ILD layer and within the trench and trench via (i.e., the "inlaid structure") formed in the ILD layer, the barrier material, which can also serve to increase adhesion, is typically formed on the dielectric surface. A conventional example of the barrier layer is Ta or its nitride deposited on the surface of the ILD layer prior to the deposition of copper as the metal interconnect layer.

#### Brief Summary Text - BSTX (12):

The conventional process for the formation of the barrier layer in dual or single inlaid copper interconnects is to form a continuous Ta or TaN film, i.e. a barrier layer or film, on the ILD using a noble gas plasma to sputter metal atoms from a Ta target onto a semiconductor device substrate. The forming of Ta or TaN as a barrier layer is determined by the gas(es) in the vacuum vessel ("gas ambient") in which the barrier layer formation occurs. For example, the conventional barrier layer for inlaid copper interconnects is formed using tantalum and argon gas combination or tantalum, argon and nitrogen gas combination in the presence of a plasma energized (sustained) by electric energy applied to the Ta sputter electrode. Alternatively, in addition to the Ta sputter electrode, other electrodes can be energized to assist (sustain) the plasma and direct ions. Examples of these are: power can be applied to the device substrate electrode to assist ion collection and a third electrode positioned to the periphery, but not between the Ta target and substrate, can be energized to increase the quantity of charged ions. The three power sources are identified as a metal sputtering DC power source, a radio frequency AC power source, and a wafer bias radio frequency power source. The resulting wafer from the process has a Ta or tantalum nitride surface portion, formed

atop the dielectric material. This tantalum nitride or Ta surface atop the dielectric serves as a barrier layer for a next metal layer of copper deposited over the dielectric layer.

Drawing Description Text - DRTX (4):

FIG. 2 includes an illustration of a prior art radio frequency pre-cleaning device;

Detailed Description Text - DETX (12):

Prior to sputtering metal onto the semiconductor substrate device 304, an adhesion region is formed atop a dielectric layer of the semiconductor substrate device 304. The adhesion region of the semiconductor substrate device 304 is formed by turning off or otherwise de-energizing the power source 314 to the metal target 312 (i.e., the refractory metal target), while maintaining the power on or otherwise energizing the rf power source 310, the radio frequency bias power source 306, or both. Simultaneously, a treating gas or treating gas/noble gas mixture such as, for example, plasma of nitrogen or an argon-nitrogen mix, is fed to the vacuum enclosure 302 from the argon gas supply 318 and the nitrogen gas supply 320 through the gas manifold 316. The nitrogen, or argon and nitrogen mix, as the case may be, is fed in quantities of approximately about 65 sccm, at temperatures of approximately about 100 C, and pressures of approximately about 40 mT, or in such other quantities, temperatures and pressures as are appropriate to obtain similar results. A plasma of the nitrogen, or argon-nitrogen mix, forms within the vacuum enclosure 302 and is maintained in the vicinity of the semiconductor substrate device 304 surface for approximately about 3 seconds or such other time period as is appropriate to obtain similar results.

Detailed Description Text - DETX (13):

The energized treating gas ions (that is, the excited gas) of the nitrogen plasma, or alternatively argon and nitrogen mix, form a silicon

dioxide:**nitrogen** (SiO.sub.2 :N) adhesion region or interlayer within the surface of the dielectric layer. This thin adhesion/interlayer region of treated ILD serves as an adhesion interface, and provides improved results for adhesion function at the surface of the dielectric layer. After the adhesion/interlayer region is formed in such manner, a barrier layer of refractory metal, such as, for example, tantalum, titanium, or tungsten, is sputtered onto the surface of the semiconductor substrate device 304. The barrier layer conforms to the topography of the vias and trenches for interconnect structures formed in the dielectric layer. The physical structures of the semiconductor device substrates 104, 204, and 304, as well as the resulting semiconductor device substrate from the adhesion/interlayer region formation and the barrier layer deposition process, are hereafter described in more detail.

#### Detailed Description Text - DETX (15):

The ILD layer 404 includes a trench 408, formed by etching of the ILD layer 404 or other conventional techniques. Within the trench 408, a via opening 406 is formed through the ILD layer 404 to the conductive layer 402. The via opening 406, like the trench 408, is formed in conventional manner, such as through successive process steps like resist spin, photolithography, etching, polishing, or other conventional steps, as those skilled in the art will know and appreciate.

#### Detailed Description Text - DETX (16):

Referring to FIG. 5, in conjunction with FIGS. 1 and 2, after degassing of the semiconductor substrate device 104 having the interconnect structure 400 via the device 100 of FIG. 1 and also after radio frequency precleaning via the cleaning device 200 of FIG. 2, an adhesion/interlayer region 410 is formed on a surface 404a of the ILD layer 404. The interconnect structure 400 of FIG. 4, after formation of the adhesion/interlayer region 410, is identified as interconnect structure 500 in FIG. 5. The adhesion/interlayer region 410 of the interconnect structure 500 is formed at a point in processing of the

semiconductor substrate device 104 after precleaning, if precleaning steps are applicable, but before barrier layer deposition within the interconnect structure 500. The adhesion/interlayer region 410 can, for example, be formed at any time in the manufacture sequence after degassing and, if applicable, precleaning, but before barrier layer deposition, for example, while the semiconductor substrate device 104 is located in the radio frequency preclean apparatus 200, in the metal deposition chamber 300, or in some other vacuum enclosure (not shown in detail) in other physical locations.

Detailed Description Text - DETX (17):

In any event, the adhesion/interlayer region 410 is formed by flowing a treating gas, such as **nitrogen**, either alone or in combination with other gas(es), such as **argon** or other gas, concurrently with at least one electrode energized, but not the Ta (i.e., metal target) electrode, to initiate and sustain a **plasma**. For example, combinations of power sources (other than the target electrode) are possible in the flowing of the treating gas, such as the **rf** power source 206 or 310 in combination with the plate power source 208 or the bias power source 306, respectively, depending whether the device 304 is located in the preclean device 200, the **sputtering** chamber 300, or elsewhere. This formation of the adhesion/interlayer region 410 creates a physical matrix of dielectric incorporated with treating gas atoms into a depth of the surface 404a of the dielectric material of the dielectric layer 404.

Detailed Description Text - DETX (25):

In other alternatives, the dielectric of the dielectric layer can be any of a wide variety of materials. The gases employed to form the adhesion/interlayer region must be varied, according to the make-up of the dielectric material. For example, the dielectric could be a modified silicon dioxide, such as silicon dioxide which is deposited a manner to create physical voids in the material, a chemically modified silicon dioxide (e.g., CVD films), various **organic** polymers, and other combinations and compositions. In such instances, nitrogen or other treating gases can be employed with additional or

alternative gases to argon and other noble gases, such as, for example, acetylene, ammonia or other gases that are suitable as a source of carbon.

Claims Text - CLTX (6):

flowing argon into the sputtering chamber while the rf power source is activated and the tantalum target is energized.

Claims Text - CLTX (10):

prior to applying tantalum to the inlaid structure, treating the inlaid structure with a plasma gas containing an element selected from nitrogen, carbon, and hydrogen while the semiconductor wafer is biased by an energized wafer bias source; and

Claims Text - CLTX (14):

7. The method of claim 6, wherein the plasma gas is nitrogen.

	<input type="checkbox"/>	<input checked="" type="checkbox"/>	1	Document ID	Issue Date	Pages	Title	Current OR	Current xRef	Retrieval Classif
1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20030024902 A1	20030206	14	Method of plasma etching low-k dielectric materials	216/67		204/192.22 ; 204/192.32	
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 20020162736 A1	20021107	11	Method of forming low resistance vias	204/192.12		216/67 ; 216/78 ; 216/79 ; 438/485 ; 438/582 ; 438/785 ; 438/9	
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6562416 B2	20030513	10	Method of forming low resistance vias	427/534		204/192.32 ; 204/192.35 ; 427/576 ; 438/479 ; 438/622 ; 438/653 ; 438/714 ; 438/720 ; 438/734	
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6511575 B1	20030128	42	Treatment apparatus and method utilizing negative hydrogen ion			204/298.34 ; 204/298.36	
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6492272 B1	20021210	9	Carrier gas modification for use in plasma ashing of photoresist	438/690		134/1.2 ; 204/192.32 ; 216/67 ; 438/725	
6	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6451673 B1	20020917	10	Carrier gas modification for preservation of mask layer during plasma etching	438/513		438/714	

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1	Li, Si Yi et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 20030024902	<input type="checkbox"/>
2	Ngo, Minh Van et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 20020162736	<input type="checkbox"/>
3	Ngo, Minh Van et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6562416	<input type="checkbox"/>
4	Shindo, Haruo et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6511575	<input type="checkbox"/>
5	Okada, Lynne A. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6492272	<input type="checkbox"/>
6	Okada, Lynne A. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6451673	<input type="checkbox"/>

	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Document ID	Issue Date	Pages	Title	Current OR	Current Xref	Retrieval Classif
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6440863 B1	20020827	14	Plasma etch method for forming patterned oxygen containing plasma etchable layer	438/710	438/711; 438/717; 438/723	
8	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6277756 B1	20010821	13	Method for manufacturing semiconductor device	438/700	257/E21.54 5; 438/243; 438/44; 438/444	
<del>9</del>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6013574 A	20000111	11	Method of forming low resistance contact structures in vias arranged between two levels of interconnect lines	438/622	257/E21.25 ; 257/E21.25 6; 257/E21.58 5; 438/625; 438/627; 438/637; 438/714; 438/722; 438/725	
<del>10</del>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5942446 A	19990824	14	Fluorocarbon polymer layer deposition predominant pre-etch plasma etch method for forming patterned silicon containing dielectric layer	438/734	216/67; 216/79; 257/E21.25 2; 257/E21.25 7; 257/E21.57 7; 438/743; 438/744	
<del>11</del>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5900163 A	19990504	10	Methods for performing plasma etching operations on microelectronic structures	216/79	216/75; 257/E21.31 2; 438/719; 438/720	

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
7	Tsai, Chia-Shiun et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6440863	<input type="checkbox"/>
8	Ohara, Junji et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6277756	<input type="checkbox"/>
9	Hause, Fred N. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6013574	<input type="checkbox"/>
10	Chen, Chao-Cheng et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 5942446	<input type="checkbox"/>
11	Yi, Whi-kun et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 5900163	<input type="checkbox"/>

	<input type="checkbox"/>	<input checked="" type="checkbox"/>	Document ID	Issue Date	Pages	Titl	Current OR	Current xRef	Retrieval Classif
<del>12</del>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5872061 A	19990216	17	Plasma etch method for forming residue free fluorine containing plasma etched layers	438/705	134/1.2; 257/E21.25 2; 438/723; 438/725	
13	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5269879 A	19931214	6	Method of etching vias without sputtering of underlying electrically conductive layer	438/694	257/E21.25 2; 257/E21.57 7; 438/712; 438/728	

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
12	Lee, Shing-Long et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 5872061	<input type="checkbox"/>
13	Rhoades, Paul et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 5269879	<input type="checkbox"/>

DOCUMENT-IDENTIFIER: US 20020162736 A1

TITLE: Method of forming low resistance vias

----- KWIC -----

Abstract Paragraph - ABTX (1):

Low resistant vias are formed by sequentially treating an opening in an interlayer dielectric and the exposed surface of a lower metal feature with an NH.sub.3 plasma followed by a N.sub.2/H.sub.2 plasma, thereby removing any oxide on the metal surface and removing residual polymers or polymeric deposits generated during etching to form the opening. Embodiments include forming a dual damascene opening in a low-k interlayer dielectric exposing the upper surface of a lower Cu or Cu alloy feature, sequentially treating the opening and the upper surface of the lower metal feature with an NH.sub.3 plasma and then with a N.sub.2/H.sub.2 plasma, **Ar sputter etching**, depositing a barrier layer lining the opening, depositing a seedlayer and filling the opening with Cu or a Cu alloy.

Application Filing Date - APD (1):

**20010502**

Summary of Invention Paragraph - BSTX (9):

[0007] The dielectric constant of materials currently employed in the manufacture of semiconductor devices for an interlayer dielectric (ILD) ranges from about 3.9 for dense silicon dioxide to over 8.0 for deposited silicon nitride. In an effort to reduce interconnect capacitance, dielectric materials

with lower values of permittivity have been explored. The expression "low-k" material has evolved to characterize materials with a dielectric constant less than about 3.9, based upon a value of the dielectric constant of a vacuum as one (1). One type of low-k material that has been explored are a group of spin on or CVD siloxane materials, such as hydrogen silsesquioxane (HSQ) and methyl silsesquioxane (MSQ) and Black-Diamond.TM. dielectric available from Applied Materials, Santa Clara, Calif. and silicon-carbon-oxygen-hydrogen (SiCOH) organic dielectrics. There are several organic low-k materials, typically having a dielectric constant of about 2.0 to about 3.8, which offer promise for use as an ILD, such as FLARE 20.TM. dielectric, a poly(arylene) ether, available from Allied Signal, Advanced Micromechanic Materials, Sunnyvale, Calif. BCB (divinylsiloxane bis-benzocyclobutene) and Silk.TM. dielectric, an organic polymer similar to BCB, both available from Dow Chemical Co., Midland, Mich.

#### Summary of Invention Paragraph - BSTX (10):

[0008] In implementing Cu and/or Cu alloy damascene techniques to form interconnection patterns with dimensions in the deep sub-micron regime, particularly when employing various low-k materials, including porous oxides, such as dielectric oxides having a porosity of about 30% to about 80% and a dielectric constant (k) of about 2.0 or lower, various problems evolve which degrade the resulting semiconductor device. For example, copper readily diffuses into conventional silicon-based materials such as polysilicon, single-crystalline silicon, silicon dioxide, and low-k inorganic and organic materials. Once semiconductive silicon-based materials are Cu doped, transistors made within or in close proximity to the Cu doped silicon-based regions either cease to function properly or are significantly degraded in electrical performance.

#### Summary of Invention Paragraph - BSTX (13):

[0011] In addition, conventional practices employ an argon (Ar) sputter etching technique to round the corners of the opening to facilitate filling, to

remove surface oxides from the underlying metal feature and to remove residual contamination. However, such Ar sputter etching typically removes a portion of the upper surface of the lower Cu or Cu alloy feature which redeposits on the side surfaces of the dielectric layer defining the opening formed therein. The resulting structure would contain Cu between the subsequently deposited barrier metal and dielectric layer which ultimately penetrates the dielectric layer and eventually poisons one or more transistors of the device.

#### Summary of Invention Paragraph - BSTX (19):

[0016] According to the present invention, the foregoing and other advantages are achieved in part by a method of manufacturing a semiconductor device, the method comprising: forming an opening in a dielectric layer exposing an upper surface of a lower metal feature; and sequentially treating the opening and upper surface of the lower metal feature with: (a) a plasma containing ammonia (NH.sub.3); following by (b) a plasma containing nitrogen (N.sub.2) and hydrogen (H.sub.2).

#### Detail Description Paragraph - DETX (2):

[0021] Upon implementing conventional interconnect technology with Cu various issues are generated adversely impacting via resistance and device reliability, such as the formation of a thin film of copper oxide on the upper surface of the lower metal feature, polymeric deposits generated by anisotropic etching and redeposition of copper on the side surfaces of the interlayer dielectric. Adverting to FIG. 1, a typical dual damascene opening is schematically illustrated by reference numeral 16 and comprises an upper trench section 16B formed in dielectric layer 15 connected to a lower via opening section 16A formed in dielectric layer 13 exposing an upper surface of lower Cu feature 10 formed in dielectric layer 11. Capping layer 12 is formed between dielectric layers 11 and 13, while middle etch stop layer 14 is formed between dielectric layers 13 and 15. The upper surface of lower Cu feature 10 typically contains a thin copper oxide surface film, believed to comprise a mixture of CuO and Cu.sub.2O generated during CMP. The thin copper oxide

surface film 17 is porous and brittle in nature, thereby generating voids as well as adversely impacting the integrity of the interconnection and increasing via resistance. In addition, as a result of anisotropic etching to form the dual damascene opening 16, polymeric deposits 19 typically accumulate, as in a corner 5A, adversely impacting via resistance. Further, after forming dual damascene opening 16, Ar sputter etching, illustrated by zigzag arrows 100, is typically performed to round the exposed corners 101, 102 of dielectric layers 15, 13, respectively, and to remove oxides and contamination. The use of Ar sputter etching has been found less than completely effective for removal of contamination and oxide film 17. Moreover, during Ar sputter etching, Cu is removed from the upper surface of Cu feature 10 and redeposits as a layer 18 on the side surfaces of dielectric layer 13. The resulting structure would contain Cu between the subsequently deposited barrier metal and dielectric layer 13, which redeposited Cu would ultimately penetrate dielectric layer 13 and eventually poison one or more transistors of the device.

Detail Description Paragraph - DETX (3):

[0022] The present invention addresses and solves high via resistance and problems attendant upon fabricating multi-layer interconnect semiconductor devices, particularly employing low-k materials to reduce parasitic RC time delays, when implementing Cu interconnect technology. The present invention particularly addresses and solves the above problems by providing efficient, cost effective methodology to decrease via resistance. Moreover, embodiments of the present invention enable formation of Cu interconnects using low-k materials employing methodology which effectively cleans the upper surface of the lower Cu metal feature of oxide, and effectively removes polymeric deposits generated during CMP, thereby enabling a significant reduction in the time required for Ar sputter etching and, consequently eliminating or significantly reducing redeposition of Cu on the side surfaces of the dielectric layer.

Detail Description Paragraph - DETX (4):

[0023] In accordance with embodiments of the present invention, a dual

damascene structure is formed in dielectric layers, such as low-k dielectric layers, e.g., F-TEOS, SiCOH or a Black-diamond.TM. dielectric. Either via first--trench last or trench first--via last damascene techniques can be employed to form the dual damascene structure. After forming the dual damascene structure, embodiments of the present invention include strategically treating the opening and upper surface of the lower Cu feature with a NH.sub.3 plasma and subsequently with a N.sub.2/H.sub.2 plasma. Such sequential treatments with an NH.sub.3 plasma followed by a N.sub.2/H.sub.2 plasma chemically reduce any copper oxide formed on the upper surface of the lower Cu feature and remove residual polymeric deposits at the bottom of the via opening, thereby significantly reducing via resistance, e.g., by as much as 25%. Moreover, the strategic sequential plasma treatments in accordance with the present invention significantly reduce the amount of time required for Ar sputter etching, e.g., by about 50%, thereby eliminating or substantially reducing Cu redeposition on the side surface of the dielectric layer defining the via. The resulting Cu interconnect structure exhibits significantly improved reliability, improved electromigration resistance and, significantly, a dramatic decrease in via resistance.

Detail Description Paragraph - DETX (7):

[0026] Subsequent processing in accordance with embodiments of the present invention comprise Ar sputter etching, as schematically illustrated by zigzag arrows 400 in FIG. 4, to round the corners 23A and 25A of low-k dielectric layers 23 and 25, respectively. Advantageously, as a result of the previous sequential NH.sub.3 and N.sub.2/H.sub.2 plasma treatments, the duration of the Ar sputter etching 400 is significantly reduced, as by about 50%, thereby eliminating or significantly reducing any redeposition of Cu from Cu feature 20 on the side surfaces of low-k dielectric layer 23. Subsequent processing in accordance with embodiments of the present invention include depositing a barrier layer or layers, such as a TaN layer 50, a Ta layer 51, and a seedlayer 52, followed by electrodeposition or electroless deposition of Cu 53 to form a dual damascene structure comprising Cu via 53B electrically connected to lower Cu feature 20 and in contact with upper Cu feature or line 53A. CMP is then

conducted to planarize the upper surface and a capping layer 54, such as silicon nitride or silicon carbide, is deposited.

Detail Description Paragraph - DETX (8):

[0027] In accordance with embodiments of the present invention, the conditions for plasma treatment and **Ar sputter etching** can be optimized in a particular situation. For example, it was found suitable to conduct the NH.sub.3 plasma treatment at an NH.sub.3 flow rate of about 130 to about 430 sccm, a N.sub.2 flow rate of about 5,000 to about 9,000 sccm, a pressure of about 2.8 to about 6.8 Torr and an RF power of about 100 to about 300 watts for a period of about 10 seconds to about 40 seconds. It was also found suitable to conduct the N.sub.2/H.sub.2 plasma treatment at a H.sub.2 flow rate of about 150 to about 350 sccm, a N.sub.2 flow rate of about 2,000 to about 8,000 sccm, a pressure of about 2.8 to about 6.8 Torr and an RF power of about 150 to about 550 watts, as for a period of about 10 to about 40 seconds.

Detail Description Paragraph - DETX (9):

[0028] In addition, as a result of the NH.sub.3 and N.sub.2/H.sub.2 plasma treatments, it was found suitable to conduct **Ar sputter etching at an Ar flow** rate of about 4 to about 6 sccm, e.g., about 5 sccm; a source RF power of about 180 to about 220 watts, e.g.; about 200 watts, and a wafer RF power of about 180 to about 200 watts, e.g., about 200 watts, for a period of time of about 4 to about 6 seconds, which constitutes a 50% reduction in the amount of time conventional employed, i.e., about 8 to about 12 seconds. As a result, Cu redeposition is avoided or substantially reduced, thereby significantly improving device reliability.

Detail Description Paragraph - DETX (10):

[0029] A wide variety of low-k materials can be employed in accordance with embodiments of the present invention, both **organic** and inorganic. Suitable **organic** materials include various polyimides and BCB. Other suitable low-k

dielectrics include poly(arylene)ethers, poly(arylene)ether azoles, parylene-N, polyimides, polynaphthalene-N, polyphenyl-quinoxalines (PPQ), polyphenyleneoxide, polyethylene and polypropylene. Other low-k materials suitable for use in embodiments of the present invention include FO.sub.x.TM. (HSQ-based), XLK.TM. (HSQ-based), and porous SILK.TM., an aromatic hydrocarbon **polymer** (each available from Dow Chemical Co., Midland, Mich.); Coral.TM., a carbon-doped silicon oxide (available from Novellus Systems, San Jose, Calif.), Black-Diamond.TM. dielectrics, Flare.TM., an **organic polymer**, HOSP.TM., a hybrid sioloxane-**organic polymer**, and Nanoglass.TM., a nanoporous silica (each available from Honeywell Electronic Materials) and halogen-doped (e.g., fluorine-doped) silicon dioxide derived from tetraethyl orthosilicate (TEOS), fluorine-doped silicate glass (FSG), and SiCOH.

Claims Text - CLTX (2):

1. A method of manufacturing a semiconductor device, the method comprising: forming an opening in a dielectric layer exposing an upper surface of a lower metal feature; and sequentially treating the opening and upper surface of the lower metal feature with: (a) a plasma containing ammonia (NH.sub.3); followed by (b) a **plasma** containing **nitrogen** (N.sub.2) and hydrogen (H.sub.2).

Claims Text - CLTX (12):

11. The method according to claim 5, comprising sequentially: forming a photoresist mask on the dielectric layer; anisotropically etching to form the opening; stripping the photoresist mask; solvent cleaning the opening; treating the opening and the upper surface of the lower metal feature with the NH.sub.3 plasma and then the N.sub.2/H.sub.2 plasma; and **argon (Ar) sputter etching** to remove residual contamination from the opening.

Claims Text - CLTX (13):

12. The method according to claim 11, comprising **Ar sputter etching** at: an **Ar** flow rate of about 4 to about 6 sccm; a source RF power of about 180 to

about 220 watts; and; a wafer RF power of about 180 to about 220 watts, for about 4 to about 6 seconds.

US-PAT-NO: 6492272

DOCUMENT-IDENTIFIER: US 6492272 B1

TITLE: Carrier gas modification for use in  
plasma ashing of photoresist

----- KWIC -----

Application Filing Date - AD (1):

20010315

Brief Summary Text - BSTX (11):

Referring particularly to FIG. 1, precursor structure 1 is of conventional structure and includes a lower metal feature 11, e.g., of copper (Cu) or a Cu-based alloy, in-laid within a first, or lower, ILD layer 10 overlying a substrate (not shown in the figure for illustrative simplicity), typically a monocrystalline Si wafer. Precursor structure 1 further comprises a thin nitride layer 14, typically a silicon nitride (Si.sub.x N.sub.y) layer from about 300-1000 .ANG. thick, e.g., about 500 .ANG. thick, formed, as by conventional techniques, to overlies the ILD layer 10 and its in-laid metal feature 11. Second, or upper ILD layer 12 is formed, as by conventional deposition techniques, to overlies the thin nitride layer 14. In this context, portion 14' of thin nitride layer 14 overlying metal feature 11 serves both as an etch stop layer during patterning of the second, upper ILD layer 12 to form a desired opening 15 therein as part of the metallization process, and as a protective layer for preventing deleterious reaction of the metal feature 11,

e.g., oxidation, nitridation, etc., during processing antecedent to filling the opening with a metal material, e.g., during reactive plasma etching of the second, upper ILD layer 12 to form opening 15.

Organic-based photoresist layer 13 formed over the second, upper ILD layer 12 and patterned by conventional photolithographic masking and etching techniques serves as an etch mask during the reactive plasma etching.

Brief Summary Text - BSTX (12):

Adverting to FIG. 1(B), subsequent to formation of opening 15 in second, upper ILD layer 12, according to conventional processing methodology, the patterned photoresist mask is then removed by means of a plasma ashing process, typically utilizing an oxygen ( $O_{2}$ ) or nitrogen ( $N_{2}$ )-based plasma (or a mixed  $O_{2}$  /  $N_{2}$  or  $N_{2}$  /  $H_{2}$  plasma) with admixed argon (Ar) gas functioning as an inert carrier gas/diluent for the  $O_{2}$ ,  $N_{2}$ ,  $O_{2}$  /  $N_{2}$ , or  $N_{2}$  /  $H_{2}$ .

Brief Summary Text - BSTX (13):

As utilized herein, the term "plasma ashing" designates plasma processes for removing organic-based photoresists, e.g., subsequent to their use as etch masks, etc. By way of illustration only, a typical  $O_{2}$ -based plasma ashing reaction is conducted (in a suitable reactor) between a carbon (C)- and hydrogen (H)-containing photoresist material generally designated by the formula  $C_{x}H_{y}$ , and plasma-activated oxygen species, generally designated as  $O^{*}$ . according to the following equation, in which each of the reaction products is volatile and thus readily removed from the reactor chamber:

Brief Summary Text - BSTX (15):

As indicated above, the active plasma ashing gases, e.g., O.sub.2, N.sub.2, O.sub.2 /N.sub.2, or N.sub.2 /H.sub.2 mixtures, are frequently supplied to the interior space of the plasma reactor admixed with inert argon (Ar) gas as a carrier gas/diluent, in order to facilitate plasma formation and moderate the plasma ashing reaction. However, as indicated in FIG. 1(B), argon ions (Ar.sup.+) generated in the ashing plasma bombard the exposed surfaces of the precursor structure 1 to sputter etch the exposed surfaces thereof at various etching rates, depending upon the particular material. However, inasmuch as the portion of the nitride etch stop/protective layer 14 exposed at the bottom of opening 15 is initially very thin, typically only about 500 .ANG. thick, any loss of thickness thereof arising from sputter etching by Ar.sup.+ ions during plasma ashing of the photoresist layer 13 for removal thereof, is problematic from the viewpoint of the requirement for maintaining the integrity and continuity of the thin nitride layer 14 prior to its desired removal immediately before opening 15 is filled with a metal, as in via formation.

Brief Summary Text - BSTX (24):

According to an aspect of the present invention, the foregoing and other advantages are obtained in part by a method of removing a photoresist layer from a workpiece by means of plasma ashing, comprising the steps of: (a) providing the interior space of a plasma reactor with a workpiece including at least one layer of a photoresist material on a surface thereof; (b) supplying the interior space of the reactor with a gas mixture comprising a plasma ashing gas and a carrier gas/diluent for the plasma ashing gas,

the carrier gas/diluent comprising an inert gas having an atomic weight greater than that of argon (Ar); and (c) removing the at least one layer of photoresist material from the workpiece surface by generating a plasma comprising the plasma ashing gas and the carrier gas/diluent within the interior space of the reactor by supplying electrical power thereto at a level which is less than that supplied to the reactor when utilizing Ar gas as a carrier gas/diluent for the plasma ashing gas, whereby deleterious sputter etching of the workpiece resulting from bombardment of the workpiece by the ionized carrier gas/diluent of the plasma is eliminated, or at least substantially reduced, relative to when Ar gas is utilized as the carrier gas/diluent.

Brief Summary Text - BSTX (30):

According to another aspect of the present invention, a method of manufacturing a semiconductor device comprises the sequential steps of: (a) providing a workpiece comprising: (i) a semiconductor substrate having a surface; (ii) a first dielectric layer overlying the substrate surface, (iii) at least one metal feature in-laid in the surface of the dielectric layer; (iv) a thin, protective/etch stop layer overlying the at least one in-laid metal feature and the first dielectric layer; and (v) a second dielectric layer overlying the thin, protective/etch stop layer; (b) forming a layer of a photoresist material over the surface of the second dielectric layer; (c) patterning the layer of photoresist material to define at least one opening therein at least partly overlying the at least one metal feature; (d) forming an opening extending through the second dielectric layer to the thin, protective/etch stop layer by an etching process utilizing

the patterned layer of photoresist material as an etch mask, the opening comprising a bottom surface formed by the thin, protective/etch stop layer; and (e) removing the patterned layer of photoresist material from the surface of the second dielectric layer by a plasma ashing process, comprising: (i) installing the etched workpiece within the interior space of a plasma reactor; (ii) supplying the interior space of the reactor with a gas mixture comprising a plasma ashing gas and a carrier gas/diluent for the plasma ashing gas, the carrier gas/diluent comprising an inert gas having an atomic weight greater than that of argon (Ar); and (iii) removing the patterned layer of photoresist material from the surface of the second dielectric layer by generating a plasma comprising the plasma ashing gas and the carrier gas/diluent within the interior space of the reactor by supplying electrical power thereto at a level less than that supplied to the reactor when utilizing Ar gas as a carrier gas/diluent for the plasma ashing gas, whereby deleterious sputter etching of the protective/etch stop layer forming the bottom surface of the opening in the second dielectric layer is eliminated, or at least substantially reduced, relative to when Ar gas is utilized as the carrier gas/diluent, thereby maintaining protection of the at least one in-laid metal feature from reaction with the plasma ashing gas during the plasma ashing of the patterned layer of photoresist material.

Detailed Description Text - DETX (4):

The methodology of the present invention is applicable to a plasma ashing processing for removal of a wide variety of organic-based photoresists, such as, but not limited to, Shipley UV 210.TM. and UV 110.TM.,

and Sumitomo AX 655.TM., and to a variety of semiconductor processing applications/sequences wherein deleterious physical sputtering of the workpiece and/or various constituent layers thereof must be avoided or at least minimized. For example, the present invention may be utilized in metallization processing utilizing dual-damascene techniques for plasma ashing of photoresist layers utilized in forming openings in ILD layers. Referring to FIG. 2(B), a dual-damascene workpiece 2 comprises an underlying metal feature 21 formed in a first, or lower ILD layer 20 overlying a semiconductor substrate (not shown for illustrative simplicity), e.g., a monocrystalline Si wafer, a thin nitride layer 14, analogous to nitride layer 14 of FIG. 1 and functioning as an etch stop/protective layer for the underlying metal feature 21, and a second, or upper ILD layer 22 having a dual damascene opening 24 comprising an upper, wider portion 24U and a lower, narrower portion 24L formed therein. Opening 24 in upper ILD layer 22 is formed by conventional photolithographic patterning and etching techniques utilizing a patterned photoresist layer similar to photoresist layer 13 utilized in forming the single-damascene opening of FIG. 1, which photoresist layer is removed by plasma ashing according to the invention. The resultant structure shown is shown in FIG. 2(B), wherein it is apparent that little or no deleterious physical sputtering of the thin nitride layer occurs when an inert carrier gas/diluent having a higher atomic weight than Ar is utilized and the plasma power is maintained at a level less than that utilized with Ar.

Claims Text - CLTX (1):

1. A method of removing a photoresist layer from a

workpiece by means of plasma ashing, comprising the steps of: (a) providing the interior space of a plasma reactor with a workpiece including at least one layer of a photoresist material on a surface thereof; (b) supplying said interior space of said reactor with a gas mixture comprising a plasma ashing gas and a carrier gas/diluent for said plasma ashing gas, said carrier gas/diluent comprising an inert gas having an atomic weight greater than that of argon (Ar); and (c) removing said at least one layer of photoresist material from said workpiece surface by generating a plasma comprising said plasma ashing gas and said carrier gas/diluent within said interior space of said reactor by supplying electrical power thereto a level less than that supplied to said reactor when utilizing Ar gas as a said carrier gas/diluent for said plasma ashing gas, whereby deleterious sputter etching of said workpiece resulting from bombardment of said workpiece by ions of said carrier gas/diluent formed in said plasma is eliminated, or at least substantially reduced, relative to when Ar gas is utilized as said carrier gas/diluent.

Claims Text - CLTX (12):

12. A method of manufacturing a semiconductor device, comprising the sequential steps of: (a) providing a workpiece comprising: (i) a semiconductor substrate having a surface; (ii) a first dielectric layer overlying said substrate surface; (iii) at least one metal feature in-laid in the surface of said dielectric layer; (iv) a thin, protective/etch stop layer overlying said at least one in-laid metal feature and said first dielectric layer; and (v) a second dielectric layer overlying said thin, protective/etch stop layer; (b) forming a layer of a photoresist material over the surface

of said second dielectric layer; (c) patterning said layer of photoresist material to define at least one opening therein at least partly overlying said at least one metal feature; (d) forming an opening extending through said second dielectric layer to said thin, protective/etch stop layer by an etching process utilizing said patterned layer of photoresist material as an etch mask, said opening comprising a bottom surface formed by said thin, protective/etch stop layer; and (e) removing said patterned layer of photoresist material from said surface of said second dielectric layer by a plasma ashing process, comprising: (i) installing the etched workpiece within the interior space of a plasma reactor; (ii) supplying said interior space of said reactor with a gas mixture comprising a plasma ashing gas and a carrier gas/diluent for said plasma ashing gas, said carrier gas/diluent comprising an inert gas having an atomic weight greater than that of argon (Ar); and (iii) removing said patterned layer of photoresist material from said surface of said second dielectric layer by generating a plasma comprising said plasma ashing gas and said carrier gas/diluent within said interior space of said reactor by supplying electrical power thereto at a level less than that supplied to said reactor when utilizing Ar gas as a said carrier gas/diluent for said plasma ashing gas, whereby deleterious sputter etching of said protective/etch stop layer forming said bottom surface of said opening in said second dielectric layer is eliminated, or at least substantially reduced, relative to when Ar gas is utilized as said carrier gas/diluent, thereby maintaining protection of said at least one in-laid metal feature from reaction with said plasma ashing gas during said plasma ashing of said patterned layer of photoresist

material.

US-PAT-NO: 6440863

DOCUMENT-IDENTIFIER: US 6440863 B1

TITLE: Plasma etch method for forming  
patterned oxygen  
containing plasma etchable layer

----- KWIC -----

Detailed Description Text - DETX (28):

Referring now to FIG. 5, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. 4a. Shown in FIG. 5 is a schematic cross-sectional diagram of a microelectronics fabrication otherwise equivalent to the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. 4a, but wherein the blanket second hard mask layer 38 has been patterned to form the patterned second hard mask layers 38a and 38b while employing a first etching plasma 42, in conjunction with the patterned photoresist layers 40a and 40b as a first etch mask layer. Within the second preferred embodiment of the present invention when the blanket second hard mask layer 38 is preferably formed of a hard mask material selected from the group of hard mask materials including but not limited to silicon oxide hard mask materials, silicon nitride hard mask materials and silicon oxynitride hard mask materials, the first etching plasma 42 preferably employs an etchant gas composition which upon plasma activation provides an active fluorine containing etchant species. More preferably, the

first etching plasma 42 employs an etchant gas composition comprising a fluorocarbon, such as but not limited to a perfluorocarbon or a hydrofluorocarbon, or alternatively sulfur hexafluoride or nitrogen trifluoride, along with an optional sputter gas component such as but not limited to argon or xenon. The first etching plasma 42 may be employed within a magnetically enhanced reactive ion etch (MERIE) method or a high density plasma reactive ion etch (HDP-RIE) method. High density plasma reactive ion etch (HDP-RIE) methods typically employ the sputtering component.

L Number	Hits	Search Text	DB	Time stamp
1	78	(((((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer)	USPAT; US-PGPUB	2003/05/30 12:14
2	3	((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	EPO; JPO; DERWENT; IBM TDB	2003/05/30 12:19
3	0	((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	EPO; JPO; DERWENT; IBM TDB	2003/05/30 12:19
4	28	((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	USPAT; US-PGPUB	2003/05/30 12:26
5	24	(((((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer))	USPAT; US-PGPUB	2003/05/30 12:20
6	4	((sputter or sputtering) with cleaning with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	USPAT; US-PGPUB	2003/05/30 13:29
7	0	(((((sputter or sputtering) with cleaning with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer)))	USPAT; US-PGPUB	2003/05/30 12:27
8	82	((sputter or sputtering) with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)	USPAT; US-PGPUB	2003/05/30 12:27
9	73	(((((sputter or sputtering) with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer)))	USPAT; US-PGPUB	2003/05/30 12:27
10	59	(((((sputter or sputtering) with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer)))) and (cleaning or etching)	USPAT; US-PGPUB	2003/05/30 12:27

*V. exhaustive search*

11	48	((((sputter or sputtering) with RF) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with cleaning) same (argon or He or Ar)) and (plasma with nitrogen) and (organic or polymer)) not (((sputter or sputtering) with etching) same (argon or He or Ar)) and (plasma with nitrogen)) and @ad<=20010510) and (organic or polymer)))) and (cleaning or etching)) and @ad<=20010510	USPAT; US-PGPUB	2003/05/30 14:03
12	1	("6518191").PN.	USPAT; US-PGPUB	2003/05/30 14:02
13	1892	(plasma with (Ar or argon) with nitrogen)	USPAT; US-PGPUB	2003/05/30 14:03
14	510	((plasma with (Ar or argon) with nitrogen)) and rf and (cleaning or etching)	USPAT; US-PGPUB	2003/05/30 14:03
15	389	((plasma with (Ar or argon) with nitrogen)) and rf and (cleaning or etching)) and @ad<=20010510	USPAT; US-PGPUB	2003/05/30 14:03
16	25	(((plasma with (Ar or argon) with nitrogen)) and rf and (cleaning or etching)) and @ad<=20010510) and ((orgainc or polymer) same dielectric)	USPAT; US-PGPUB	2003/05/30 14:04

US-PAT-NO: 6284657

DOCUMENT-IDENTIFIER: US 6284657 B1

TITLE: Non-metallic barrier formation for copper damascene type interconnects

----- KWIC -----

Application Filing Date - AD (1):  
20000225

Brief Summary Text - BSTX (14):

A fourth object of this invention is to provide a method for preventing conducting materials, such as copper, sputtered onto the sidewalls of trenches and vias during etching, from diffusing into surrounding dielectric materials.

Drawing Description Text - DRTX (12):

FIG. 11 illustrates the design parameters that must be considered in forming a dual-damascene type interconnect in a 0.15 micron and beyond generation of microelectronic fabrications such as is illustrated in FIG. 10. The figure also is a schematic cross-sectional view of the patterning and etching of the dual-damascene trench and via in accordance with the method of the present invention.

Detailed Description Text - DETX (7):

FIG. 2 is a schematic cross-sectional view of the fabrication shown in FIG. 1 subsequent to the patterning and etching of a dual-damascene interconnect formation consisting of a trench (22) and a via (24), which is open to the Cu layer (10). The width of said trench is between 0.25 microns and 2.0 microns, the width of said via is between 0.15 microns and 0.40 microns. The etching process consists of plasma-assisted dry etching wherein the etching chemistry comprises one or more of the following: fluorocarbons (eg. CF.sub.4, C.sub.4 F.sub.8), hydrocarbons, fluorine substituted hydrocarbons (eg. CHF.sub.3), fluorosulfurs (eg. SF.sub.6), chlorine, hydrogen bromide, oxygen, nitrogen, argon, hydrogen and carbon monoxide, wherein the choice of chemistries is tailored appropriately to the nature of the different layers.

Detailed Description Text - DETX (11):

FIG. 6 shows a schematic cross-sectional view of the same microelectronics fabrication of FIG. 5, subsequent to an anisotropic etch used to form a spacer layer (19) from the non-metallic layer (shown as (15) in FIG. 5). Said anisotropic etch consists of a plasma-assisted etch wherein the etching chemistry comprises one or more of the following: chlorine, boron trichloride, oxygen, hydrogen, nitrogen, forming gas (a mixture of nitrogen and hydrogen), fluorocarbon(s), fluorine-substituted hydrocarbon(s) and argon. As is seen in the figure, the etch has removed the non-metallic layer material (shown as (15) in FIG. 5) from the capping layer surface (17), partially removed said non-metallic layer material from the etch-stop layer surface (21) and partially removed said non-metallic layer material from the passivation layer surface (13), leaving said non-metallic layer material on the vertical surfaces of the trench and via formation (19) as shown.

Detailed Description Text - DETX (12):

FIG. 7 is a schematic cross-sectional view of the same microelectronics fabrication of FIG. 6, subsequent to a further etching which removes (at (21)) the passivation layer (12) from the conducting layer (10) beneath it. The etching process consists of plasma-assisted etching wherein the etching

chemistry comprises one or more of the following: fluorocarbons (eg. CF.sub.4, C.sub.4 F.sub.8), hydrocarbons, fluorine substituted hydrocarbons (eg. CHF.sub.3), oxygen, nitrogen, argon, and hydrogen. Note that during the **etching** process there is some degree of penetration into the conducting layer (21). During this process, the barrier layer now also acts as a protective layer to prevent diffusion of the sputtered conductor and its oxides into the surrounding dielectric, which is particularly important if the conductor is copper.

Detailed Description Text - DETX (13):

FIG. 8 is a schematic cross-sectional view of the same microelectronics fabrication of FIG. 7, subsequent to the wet or dry **cleaning** of the sputtered conductor (not shown) and the formation of a metallic barrier layer (22), which comprises a layer of, but is not restricted to, TaN, TiN, WN, or tantalum or metal-silicon-nitride, of thickness between 50 angstroms and 2,000 angstroms. The fabrication is now ready for the insertion of a conducting inlay, typically a copper inlay formed by the deposition of copper over all surfaces of said trench and via formation (not shown).

Detailed Description Text - DETX (19):

FIG. 10 is a schematic cross-sectional view of a microelectronics fabrication, including a microelectronics fabrication of the below 0.15 micron device generation, within which a dual-damascene interconnect is to be formed. The fabrication comprises a conducting layer (10), which is typically a copper (Cu) conducting layer or a composite stack comprising one or more of the following metals: titanium, tungsten, titanium nitride and aluminum-copper, of thickness between 2,000 angstroms and 15,000 angstroms on which has been formed a passivating layer (12), which could be a layer of silicon nitride (SiN) or BLOK (mfg. by Applied Materials Corp.), of thickness between 500 angstroms and 5,000 angstroms, on which has been formed a first **dielectric** layer (14), which could be a layer of SiO.sub.2 or doped SiO.sub.2 such as PSG or a layer of carbon-doped silicon oxide such as methylsilsequioxane or a layer of low

dielectric constant (low-k) organic polymer such as FLARE (mfg. by Allied Signal Corp.), SILK (mfg. by Dow Chemical Corp.), or a layer of inorganic polymer such as hydrogen silsesquioxane or a layer comprising the porous entity of the aforementioned dielectric films, of thickness between 1,000 angstroms and 10,000 angstroms, on which has been formed an etch-stop layer (16), which could be a layer of silicon carbide, SiN, SiON, or BLOK (mfg. by Applied Materials Corp.), of thickness between 500 angstroms and 5,000 angstroms, on which has been formed a second layer of dielectric material (18), similar to the first layer and on which has been formed an optional capping layer (20), which could be a layer of SiN of thickness between 500 angstroms and 5,000 angstroms.

Detailed Description Text - DETX (20):

FIG. 11 is a schematic cross-sectional view of a trench and via formation that has been patterned and etched according to either a trench first, via first or self-aligned scheme. The etching process consists of plasma-assisted dry etching wherein the etching chemistry comprises one or more of the following: fluorocarbons (eg. CF.sub.4, C.sub.4 F.sub.8), hydrocarbons, fluorine substituted hydrocarbons (eg. CHF.sub.3), fluorosulfurs (eg. SF.sub.6), chlorine, hydrogen bromide, oxygen, nitrogen, argon, hydrogen and carbon monoxide, wherein the choice of chemistries is tailored appropriately to the nature of the different layers. The dashed lines (17) indicate the design parameters for the final copper inlay, allowing for the thickness of the usual barrier layer. The solid vertical lines indicate the actual etched surface dimensions which are required to fulfill those design parameters. The trench is etched through the optional capping layer (20) and the second dielectric layer (18), stopping at the etch-stop layer (16). The via is etched through to the passivation layer (12).

Detailed Description Text - DETX (22):

FIG. 13 shows a schematic cross-sectional view of the fabrication in FIG. 12 subsequent to an anisotropic etch of the carbon-based layer to form a spacer

layer (19). Said anisotropic etch consists of a plasma-assisted etch wherein the **etching** chemistry comprises one or more of the following: chlorine, boron trichloride, oxygen, hydrogen, nitrogen, forming gas (a mixture of nitrogen and hydrogen), and fluorocarbon(s). The etch removes the non-metallic barrier layer from the optional capping layer (20) and partially from the etch-stop layer (16) and passivation layer (12). The carbon-based barrier layer remains on the vertical walls of the trench and via to form a spacer layer (19). The passivation layer (12) is subsequently etched to expose the underlying conductor layer (10). Said etch is a **plasma** assisted etch wherein the **etching** chemistry comprises one or more of the following: fluorocarbons, fluorine-substituted hydrocarbons, **argon and nitrogen**. There is some penetration by the etch into the conductor, hence the non-conductive barrier acts as a protective layer to prevent diffusion of the sputtered conductor and its oxides into the surrounding dielectrics.

Detailed Description Text - DETX (28):

FIG. 16 is a schematic cross-sectional view of the fabrication in FIG. 15 after a first plasma treatment of the upper surface of the first dielectric layer (14) with a nitrogen, hydrazine or NH.sub.3 plasma. Said plasma is formed in a chamber wherein a plasma can be generated by an **RF** power source (13.56 MHz, 100 W-2,000 W) or a microwave source (2.45 GHz, 100 W-2,000 W) at a pressure between 1 mTorr and 50 mTorr. The plasma treatment forms a "pseudo-carbon nitride" layer (15), indicated as a shaded region, on that upper surface, by means of the reaction:

Detailed Description Text - DETX (32):

FIG. 19 is a schematic cross-sectional view of the fabrication in FIG. 18, subsequent to the formation of an optional capping layer (20), which typically could be a layer of SiN of thickness between 500 angstroms and 5,000 angstroms and the patterning and **etching** of a dual-damascene trench (22) and via (24) formation. The passivation layer (12) has been removed by the etch, opening the via to the underlying conducting layer (10).

Claims Text - CLTX (3):

patterning and etching a trench and via structure that passes through said capping layer, said second dielectric layer, said etch-stop layer and said first dielectric layer and extends, thereby, to said passivating layer;

Claims Text - CLTX (5):

etching away portions of said non-metallic layer of fluorine diffusion resistant material to form a fluorine diffusion resistant barrier "spacer" over the side-walls of said trench and via formation;

Claims Text - CLTX (6):

etching away the exposed portion of said passivation layer to expose the conducting layer;

Claims Text - CLTX (19):

12. The method of claim 11 wherein the etch is a plasma assisted etch wherein the etching chemistry comprises one or more of the gases selected from the group consisting of: fluorocarbon(s), fluorine-substituted hydrocarbon(s), fluorosulfur, chlorine, hydrogen bromide, oxygen, nitrogen, argon, hydrogen and carbon monoxide.

Claims Text - CLTX (21):

14. The method of claim 13 wherein the etch is a plasma assisted etch wherein the etching chemistry comprises one or more of the gases selected from the group consisting of: fluorocarbon(s), fluorine-substituted hydrocarbon(s), fluorosulfur, chlorine, hydrogen bromide, oxygen, nitrogen, argon, hydrogen and carbon monoxide.

Claims Text - CLTX (23):

16. The method of claim 15 wherein the etch is a **plasma** assisted etch wherein the **etching** chemistry comprises one or more of the gases selected from the group consisting of: fluorocarbon(s), fluorine-substituted hydrocarbon(s), fluorosulfur, chlorine, hydrogen bromide, oxygen, **nitrogen**, **argon**, hydrogen and carbon monoxide.

Claims Text - CLTX (25):

18. The method of claim 1 wherein the non-metallic layer of fluorine diffusion resistant material is etched with a **plasma** assisted etch wherein the **etching** chemistry comprises one or more of the gases selected from the group consisting of: chlorine, boron trichloride, oxygen, hydrogen, **nitrogen**, forming gas (a mixture of hydrogen and **nitrogen**) fluorocarbon(s), fluorine-substituted hydrocarbon(s) and **argon**.

Claims Text - CLTX (26):

19. The method of claim 1 wherein the passivation layer is etched with a **plasma** assisted etch wherein the **etching** chemistry comprises one or more of the gases selected from the group consisting of: fluorocarbon(s), fluorine-substituted hydrocarbon(s), hydrocarbon(s), oxygen, **nitrogen** and **argon**.

US-PAT-NO:

6042929

DOCUMENT-IDENTIFIER:

US 6042929 A

TITLE:

Multilayer metalized composite on polymer film product  
and process

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Brief Summary Text - BSTX (18):

In accordance with this invention, a polymeric film-metal composite structure is provided which has a high initial peel strength between the metal and the polymeric film surface that does not significantly deteriorate after repeated high temperature thermal cycling. In the first step of the process of this invention, a plasma, preferably one containing a source of nitrogen ions, with sufficient energy, that is an energy greater than about 20 Joules/cm.sup.2 up to about 200 Joules/cm.sup.2, to roughen or create the microprofile on the polymeric film surface by reactive ion etching. The pressure utilized in the plasma chamber is less than about 1500 mTorr and more usually between about 1 and about 50 mTorr. The reactive ion plasma etch with nitrogen produces a surface microprofile with protuberances which extend from the film surface, in contrast to the smooth undulations that characterize the microprofile of a polymeric surface etched with a reactive ion plasma containing oxygen. When plasma energies less than about 20 Joules/cm.sup.2 are utilized, insufficient surface roughening occurs; on the other hand, when plasma energies above about 200 Joules/cm.sup.2 are utilized, mechanical degradation of the film surface occurs. It is believed that the improved peel strength properties of the composites of this invention result from a combination of greater mechanical adhesion afforded by the roughened microprofile of the film surface and

chemical bonding of the subsequently-applied metal nitride to nitrogen sites generated on the polymeric film surface. Although a variety of plasma gases may be utilized, the preferred plasma gas is a mixture consisting of a source of nitrogen ions, for example, nitrogen gas, ammonia, or various amines, or mixtures thereof, and an inert gas such as argon, neon, krypton, or xenon. The preferred energy source for the film-etching plasma is a radio frequency (RF) power supply but other lower frequency power sources are also suitable.

#### Detailed Description Text - DETX (11):

Based on the superior results achieved in Examples 2 and 3 with nitrogen-based processes, an evaluation was made of a new tri-layer system based on a polyimide film substrate plasma-etched in a 50/50 Ar/N.sub.2 gas mixture at about 20 J/cm.sup.2. In this case, the tri-layer construction consisted of a wider variety of metal nitride barrier layers 100 Angstroms thick, followed by a copper nitride interlayer 100 Angstrom thick, both sputter-deposited in a 50/50 Ar/N.sub.2 plasma, a third layer of pure copper metal 1000 Angstroms thick was deposited in a 100% Ar plasma.

#### Detailed Description Text - DETX (16):

Based on the results presented in Table V, it appears that, at comparable energy levels on this particular polymer substrate, the gases evaluated yield comparable results. Since it is well-known that ammonia readily degrades in a plasma to hydrogen and active nitrogen species, it is not surprising that the 50/50 argon/ammonia gas mixture in Sample 4 produced essentially the same result as Sample 3, an Ar/N.sub.2 mixture. Even a 100% nitrogen plasma (Samples 9 and 10) achieved results comparable to those obtained with neon, helium, and argon, which suggests that a noble gas is not essential. However, with a noble gas present, a plasma can be initiated at lower energy levels; consequently, Ar/N.sub.2 is the preferred gas mixture for an energy-efficient source of nitrogen ions.

Detailed Description Text - DETX (18):

Although Ar/N.sub.2 was determined to be the most effective gas mixture in the foregoing example, an additional experiment was undertaken to determine the adhesion sensitivity of metal-nitride barrier layer adhesion to plasma gas nitrogen content. Accordingly, sheets of 1 mil Kapton brand polyimide film, type E, were plasma-etched at about 20 J/cm.sup.2 with gas mixtures containing different ratios of nitrogen to argon. These samples were then metalized in a three layer construction consisting of a 100 Angstrom thick barrier layer of titanium nitride formed in the same plasma gas mixture used for the pre-treatment step, followed by 100 Angstroms of copper nitride formed in the same plasma gas mixture, followed by a 1000 Angstrom thick pure copper layer sputtered in 100% argon. As in the foregoing examples, all the sample sheets were subsequently electroplated to 35 .mu.m of copper, exposed to three thermal cycles at 180.degree. C. for 1 hr., then subjected to the IPC-TM650-Method 2.4.9, 90.degree. German wheel peel test. All peel results set forth below in Table VI are the average of at least three peel strips.

Detailed Description Text - DETX (19):

From the results summarized in Table VI, it appears that above about 5% nitrogen content, the effectiveness of Ar/N.sub.2 gas mixtures for both the plasma pre-treatment process and the barrier layer sputtering process is relatively insensitive to nitrogen content. Nevertheless, below some minimum amount, probably 5% or less by volume, insufficient nitrogen in the plasma will cause the titanium to deposit on the polymer film surface as free metal, thereby rendering it unsuitable for the applications of interest for this invention.

Detailed Description Text - DETX (21):

It is well known that plasma energy level can have an important effect on barrier layer adhesion. To investigate this relationship, sheets of 1 mil Kapton brand polyimide film, type E, were plasma-etched in a 50/50 Ar/N.sub.2 gas mixture using different energy levels. The energy levels were calculated

from the watts of **RF** energy absorbed by the plasma in the area of the sample and, by varying the time of exposure and the pressure in the vacuum chamber, ranged from 2 to 200 J/cm.sup.2. In this example, the samples were metalized in a three layer construction consisting of a 100 Angstrom thick barrier layer of nickel nitride formed in the same plasma gas mixture used for the pre-treatment step, followed by 100 Angstroms of copper nitride formed in the same plasma gas mixture, followed by a 1000 Angstrom thick pure copper layer sputtered in 100% argon. As in the foregoing examples, all the sample sheets were subsequently electroplated to 35 .mu.m of copper, exposed to three thermal cycles at 180.degree. C. for 1 hr., then subjected to the IPC-TM650-Method 2.4.9, 90.degree. German wheel peel test. All peel results set forth below in Table VII are the average of at least three peel strips.